3/4 B.Tech - FIFTH SEMESTER

EC5T3 Computer Architecture & Organization Credits: 3

Lecture: 3 periods/week **Internal Assessment: 30 Marks**
Tutorial: 1 period /week Semester **Semester End Examination: 70 Marks**

Prerequisites: Switching Theory and Logic Design (EC3T6)

Course Objectives:

- To introduce basic principles of computer organization and architecture.
- To provide examples of different processors and instruction sets.
- To give a basis for understanding issues of computer operation and performance.
- To familiarize the students with computer arithmetic.

Learning Outcomes:

Student will be able to

- Conceptualize the impact of instruction set architecture on cost-performance of computer design.
- Design a pipeline for consistent execution of instructions with minimum hazards.
- Articulate different ways to incorporate long latency operations in pipeline design.
- Analyze the impact of branch scheduling techniques and their impact on processor performance.
- Restate alternatives in cache design and their impacts on cost/performance.

UNIT-I

Register Transfer and Microoperations: Register Transfer Language, Register Transfer, Bus and Memory Transfers, Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic Logic Shift unit

Basic Computer Organization and Design: Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction cycle. Memory Reference Instructions. Input-Output and Interrupt, Complete Computer Description, Design of Basic Computer, Design of Accumulator Logic.

UNIT-II

Microprogrammed Control: Control Memory, Address Sequencing, Microprogram Example, Design of control unit.

Central Processing Unit: Introduction, General Register Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation Program control, Reduced Instruction Set Computer (RISC), Overlapped Register Windows

UNIT-III

Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access(DMA), Input- Output Processor(IOP), Serial Communication

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory

UNIT-IV

Computer Arithmetic: Introduction, Addition and Subtraction, Multiplication Algorithms, Division Algorithms for fixed, floating and BCD.

UNIT-V

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors

Learning Resources

Text Books:

1. Computer System Architecture, M. Moris Mano, 3rd Edition, Pearson/ PHI, 2007
2. Computer Architecture and Organization, John P. Hayes., 3rd Mc Graw Hill International editions, 1998.

References:

1. Computer Organization and Architecture, William Stallings 7th Edition, PHI/Pearson. 2006
2. Computer Organization, Car Hamacher, Zvonks Vranesic, Safwat Zaky, 5th Edition, McGrawHill. 2002
3. Computer Architecture: A quantitative approach, John L. Hennessy, David A. Patterson, 4th Mc Graw Hill International editions,2006.
4. Structured Computer Organization, Andrew S. Tanenbaum,4th edition, Prentice Hall , 1998

Web Resources:

1. http://nptel.iitm.ac.in/courses/Webcourse-contents/IITKANPUR/Comp Architecture/page1.htm
2. http://nptel.iitm.ac.in/courses/Webcourse-contents/IIT20Guwahati/comp_org_arc/web/index.htm
3. http://williamstallings.com/COA5e.html